REMARKS

The Office Action dated November 1, 2005, has been received and carefully noted. The above amendments and following remarks are submitted as a full and complete response thereto.

Claims 1, 3, 4, 13, 17, 18, 20-21 and 29 have been amended. The title of the invention has also been amended. Therefore, claims 1-30 are pending in the present application.

Title of the Invention

The title of the invention has been amended as suggested in the Office Action to "Memory Device and Method for Arbitrating Internal and External Access."

Rejected under 35 U.S.C. § 102(e)

Claims 1-30 were rejected under 35 U.S.C. § 102(e) as being anticipated by Mizugaki et al. (U.S. Patent No. 6,545,943, hereinafter "Mizugaki"). This rejection is respectfully traversed.

Claim 1 recites a semiconductor memory device comprising, among other features, a signal generating circuit, connected to the arbiter, for generating an internal operation signal in accordance with at least one of the first mode trigger signal and the second mode trigger signal, wherein the arbiter executes the first access mode by priority over the second access mode, when the arbiter is supplied with the first entry signal within a predetermined period after priority for the second access mode has been determined, wherein the predetermined period comprises a period from a point at which the second entry signal is enabled to a point at which a predetermined word line of the plurality of word lines is enabled in the second access mode.

Claim 18 recites a semiconductor memory device comprising, among other features, whereby in case of receiving the first entry signal within a predetermined period after having received the second entry signal, the arbiter stops executing the second access mode and executes the first access mode, wherein the predetermined period comprises a period from a point at which the second entry signal is enabled to a point at which a predetermined word line of the plurality of word lines is enabled in the second access mode.

Claim 21 recites a semiconductor memory device comprising, among other features, executing the first access mode by priority over the second access mode when the first entry signal is detected, wherein the predetermined period comprises a period from a point at which execution of the second access mode was started to a point at which a predetermined word line in the semiconductor memory device is enabled in the second access mode.

Claim 29 recites a semiconductor memory device comprising, among other features, executing the second access mode after the first access mode is finished; and measuring a period from a point at which the first entry signal is supplied to a point at which the first access mode is finished, wherein the predetermined period comprises a period from a point at which the second entry signal is enabled to a point at which a predetermined word line of the plurality of word lines is enabled in the second access mode.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Mizugaki discloses a technique for reducing the power consumption associated with word line activation in a semiconductor memory device. The semiconductor memory device of Mizugaki is provided with a word line activation controller for controlling word line activation. Where consecutive operation cycles use multiple-bit addresses that include an identical row address, the controller maintains an activated state of a word line without deactivation thereof until the row address changes. In the event of a refresh request when a word line in a certain block is in an activated state, the controller of Mizugaki can deactivate the word line, with the proviso that no external access is currently being performed in the block. Where a request for external access to the block is made within a predetermined period after the refresh request, the refresh operation for the block is suspended, and the word line for external access is activated.

In particular, Figure 15 of Mizugaki illustrates delaying a refresh operation when a bank signal (external access signal) BNK goes to H level after an external access signal #EX0 goes to H level.

However, Applicant submits that Mizugaki fails to disclose, for instance, executing a first access mode by priority over a second access mode (refresh mode), when an arbiter is supplied with a first entry from a point at which a second entry signal (refresh request signal (ref-req) is enabled to a point at which a predetermined word line of the plurality of word lines is enabled in the second access mode of the present invention. Specifically, Mizugaki fails to disclose at least the features highlighted above with respect to claims 1, 18, 21 and 29.

As such, Applicant submits that Mizugaki fails to disclose each and every element recited in claims 1, 18, 21 and 29 of the present application.

Pursuant to US patent law, in order to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Mizugaki fails to disclose or suggest each and every feature of claims 1, 18, 21 and 29. Accordingly, Applicant respectfully submit that claims 1, 18, 21 and 29 are not anticipated Mizugaki. Therefore, Applicant respectfully submits that claims 1, 18, 21 and 29 are allowable.

As claims 2-17 depend from claim 1, claims 19-20 depend from claim 18, claims 22-28 depend from claim 21, and claim 30 depends from claim 29, Applicant submits that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the above, the Applicant respectfully requests the allowance of claims 1-30 and the prompt issuance of a Notice of Allowability.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper,

may be charged to counsel's Deposit Account No. 01-2300, referencing Attorney Docket No. 108075-00114.

Respectfully submitted,

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